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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/606,586 | 06/26/2003 | David William Boerstler | AUS920020703US1 | 5097 |

45327 7590 11/18/2004

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| EXAMINER | |
|---|---|
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| ART UNIT | PAPER NUMBER |
|---|---|
| 2811 | |

DATE MAILED: 11/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/606,586 | BOERSTLER ET AL. | |
| | Examiner | Art Unit | |
| | Quang D Vu | 2811 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *26 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Election/Restrictions*

Applicant's election without traverse of group I (claims 1-15) in the reply filed on 10/26/04 is acknowledged.

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3 and 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,361,207 to Ferguson in view of US Patent No. 6,381,286 to Wilkinson et al.

Regarding claim 1, Ferguson (figure1) teaches an integrated circuit (IC) chip, comprising:

a plurality of chip (areas of chip [101]) areas;

a plurality of temperature sensors (112, 104), at least one temperature sensor per chip area (each temperature sensor is located on the difference area of chip); and

a comparator (116) for comparing the output of the plurality of temperature sensors (112, 104).

Ferguson differs from the claimed invention by not showing the comparator further employable to generate a signal if the difference between the outputs of the plurality of temperature sensors exceeds a threshold. However, Wilkinson et al. teach the comparator

outputs a signal when the difference between the outputs of the plurality of temperature sensors exceeds a threshold (column 12, lines 48-54). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Wilkinson et al. into the device taught by Ferguson in order to controls the output signals of the temperature sensors.

Regarding claim 2, the combined device shows the temperature sensor measures a temperature to generate a voltage.

Regarding claim 3, the combined device shows the temperature sensor measures a temperature to generate a current.

Regarding claim 5, the combined device shows the temperature sensor comprises a thermal resistor (Ferguson; column 3, lines 57-62).

Regarding claim 6, the combined device shows the comparator is coupled to the chip.

Regarding claim 7, the combined device shows the comparator compares voltages generated from the plurality of temperature sensors.

3. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ferguson in view of Wilkinson et al., and further in view of US Patent No. 5,159,520 to Toyooka et al.

Regarding claim 4, the disclosures of Ferguson and Wilkinson et al. are discussed as applied to claims 1-3 and 5-7 above.

The combined device differs from the claimed invention by not showing the temperature sensor comprises a pn junction. However, Toyooka et al. teach the temperature sensor comprises a pn junction (column 1, lines 32-33). Therefore, it would have been obvious to one having

ordinary skill in the art at the time the invention was made to incorporate the teaching of Toyooka et al. into the device taught by Ferguson and Wilkinson et al. because it generates a current that is related with the measured temperature.

4. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ferguson in view of Wilkinson et al., and further in view of US Patent No. 6,337,246 to Sobek et al.

Regarding claim 8, the disclosures of Ferguson and Wilkinson et al. are discussed as applied to claims 1-3 and 5-7 above.

Ferguson teaches the integrated circuit (101) and substrate (106). Ferguson and Wilkinson et al. differ from the claimed invention by not showing a layer of silicon dioxide interposed between the substrate of the integrated circuit and a computational element of the integrated circuit. However, Sobek et al. (figure 3) teach a layer silicon dioxide (24), which is interposed between the substrate (16) and integrated circuit chip gate stack. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Sobek et al. into the device taught by Ferguson and Wilkinson et al. because it protects the surface of the substrate.

5. Claims 9, 11, 12, 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,361,207 to Ferguson in view of US Patent No. 5,805,403 to Chemla.

Regarding claim 9, Ferguson (figure 1) teaches an integrated circuit, comprising:

at least two temperature sensors (112, 104), at least one temperature sensor per chip area (each temperature sensor is located on the difference area of chip); and

a comparator (116) for comparing the output of the plurality of temperature sensors.

Ferguson differs from the claimed invention by not showing at least two chip areas, at least one chip area employed as a simulation area. However, Chemla (figure 1) teaches at least two chips areas with at least two temperature sensors. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate he teaching of Chemla into the device taught by Ferguson because it reduces the cost and minimizes the step of production.

Regarding claim 11, the combined device shows a third chip area and a third associated temperature sensor, wherein the output of the third associated temperature sensor is employed by the comparator.

Regarding claim 12, the combined device shows the temperature sensor measures a temperature to generate a voltage.

Regarding claim 14, the combined device shows the temperature sensor comprises a thermal resistor (Ferguson; column 3, lines 57-62).

Regarding claim 15, the combined device shows the comparator is coupled to the chip.

6. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ferguson in view of Chemla, and further in view of US Patent No. 6,337,246 to Sobek et al.

Regarding claim 10, the disclosures of Ferguson and Chemla are discussed as applied to claims 9, 11, 12, 14 and 15 above.

Ferguson teaches the integrated circuit (101) and substrate (106). The combined device differs from the claimed invention by not showing a layer of silicon dioxide interposed between

the substrate of the integrated circuit and a computational element of the integrated circuit. However, Sobek et al. (figure 3) teach a layer silicon dioxide (24), which is interposed between the substrate (16) and integrated circuit chip gate stack. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Sobek et al. into the device taught by Ferguson and Chemla because it protects the surface of the substrate.

7. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ferguson in view of Chemla, and further in view of US Patent No. 5,159,520 to Toyooka et al.

Regarding claim 13, the disclosures of Ferguson and Chemla are discussed as applied to claims 9, 11, 12, 14 and 15 above.

The combined device differs from the claimed invention by not showing the temperature sensor comprises a pn junction. However, Toyooka et al. teach the temperature sensor comprises a pn junction (column 1, lines 32-33). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Toyooka et al. into the device taught by Ferguson and Chemla because it generates a current that is related with the measured temperature.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 571-272-1667. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

qv
November 10, 2004

Sara Crane
Primary Examiner